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In the Claims:

Please amend claims 1-2, 4-5, 8 and 10, cancel claim 7, and add new claims 11-16 as indicated below. This listing of claims replaces all prior versions.

1. (Currently Amended) A semiconductor device comprising a thermally and electrically conductive bottom plate on an upper side of which there is a semiconductor element with a first connection region and a second connection region, said regions being coupled to, respectively a first conductor and a second conductor, said semiconductor element being surrounded by an electrically insulating synthetic resin envelope that covers a side face of the bottom plate, which side face is provided with a recess that is filled with a part of the envelope, characterized in that the recess, viewed in cross-section at right angles to an edge of the bottom plate, takes the form of a staircase with at least two steps, wherein a connection region of a drain of the semiconductor element borders on the bottom plate and forms a drain connection that projects from the envelope, and wherein connection regions of a source and a gate of the semiconductor element are situated on a side of the semiconductor element opposite the connection region of the drain, and the first and second conductors form, respectively, source and gate connections that project from the envelope.

2. (Currently Amended) A semiconductor device as claimed in Claim 1, wherein the first and ~~the~~ second conductors form an assembly, of which part is coupled to, respectively, the first and ~~the~~ second connection regions, ~~which parts are also~~ said part being surrounded by ~~an~~ the electrically insulating synthetic resin envelope.

3. (Original) A semiconductor device as claimed in Claim 1, characterized in that the height of the recess at the location of the first step lies in the range between 20 and 60 μm and at the location of the second step in the range between 100 and 150 μm, while the width of the steps ranges between 0.2 and 0.4 mm.

4. (Currently Amended) A semiconductor device as claimed in Claim 1, characterized in that the device comprises a further electrically conductive bottom plate that is separated from the bottom plate and on which a further semiconductor element is situated having a first and a second further connection region, said further regions being coupled to, respectively a first further conductor and a second further conductor, said further semiconductor element being surrounded by the electrically insulating synthetic resin envelope that is connected to the further bottom plate in a way similar to the manner in which it is connected to the bottom plate.

5. (Currently Amended) A semiconductor device as claimed in Claim 4, wherein the first and second further conductors are part of ~~the~~ an assembly, of which part is coupled to the further semiconductor element[[s]], said part ~~also~~ being surrounded by the resin envelope.

6. (Previously presented) A semiconductor device as claimed in Claim 1, characterized in that the semiconductor element comprises a MOSFET transistor.

7. (Canceled)

8. (Currently Amended) A method of manufacturing a semiconductor device, comprising the steps of:
- providing an electrically conductive bottom plate having an upper side and a lower side, and a side face, at which side face a recess is present, with its lower side on a support plate;
- securing a semiconductor element on the upper side of the bottom plate, which semiconductor element is provided with a first connection region and a second connection region;
- providing an assembly of a first conductor and a second conductor, such that a part thereof is coupled to, respectively, the first and the second connection region, characterized in that the assembly of conductors and the bottom plate are formed from

two conductor frames, one of which comprises the bottom plate and a conductor, and the other one of which comprises another conductor, and after securing the semiconductor element to the bottom plate in one conductor frame, the other conductor frame is secured to the semiconductor element,

- surrounding the semiconductor element and the parts of the conductors coupled thereto by an electrically insulating synthetic resin envelope, such that it covers also the side face of the bottom plate and that it projects above the support plate in the recess, and
- removing the support plate, wherein the recess of the bottom plate has or is given the shape of a staircase with at least two steps, when viewed in a direction transverse and perpendicular to the edge of the bottom plate.

9. (Original) A method as claimed in Claim 8, wherein the recess is formed by means of a punch technique.

10. (Currently Amended) A method as claimed in Claim 8, characterized in that ~~the assembly of conductors and the bottom plate is formed from two conductor frames, one of which comprises the bottom plate and a conductor, and the other one of which comprises another conductor, and after securing the semiconductor element to the bottom plate in one conductor frame, the other conductor frame is secured to the semiconductor element,~~ after ~~which~~ the envelope is provided, ~~and~~ superfluous parts of the conductor frames are removed.

11. (New) A semiconductor device comprising

a thermally and electrically conductive bottom plate on an upper side of which there is a semiconductor element with a first connection region and a second connection region, said regions being coupled to, respectively a first conductor and a second conductor, said semiconductor element being surrounded by an electrically insulating synthetic resin envelope that covers a side face of the bottom plate, which side face is provided with a recess that is filled with a part of the envelope, characterized in that the recess, viewed in cross-section at right angles to an edge of the bottom plate, takes the form of a staircase with at least two steps; and

a further electrically conductive bottom plate that is separated from the bottom plate and on which a further semiconductor element is situated having a first further connection region and a second further connection region, said further regions being coupled to, respectively a first further conductor and a second further conductor, said further semiconductor element being surrounded by the electrically insulating synthetic resin envelope that is connected to the further bottom plate in a way similar to the manner in which it is connected to the bottom plate.

12. (New) A semiconductor device as claimed in Claim 11, wherein the first and second conductors form an assembly, of which part is coupled to, respectively, the first and second connection regions, said part being surrounded by the electrically insulating synthetic resin envelope.

13. (New) A semiconductor device as claimed in Claim 11, characterized in that a height of the recess at a location of the first step lies in a range between 20 and 60 μm and at a location of the second step in a range between 100 and 150 μm, while a width of the steps ranges between 0.2 and 0.4 mm.

14. (New) A semiconductor device as claimed in Claim 11, wherein the first and second further conductors are part of an assembly, of which part is coupled to the further semiconductor element, said part being surrounded by the resin envelope.

15. (New) A semiconductor device as claimed in Claim 11, characterized in that the semiconductor element comprises a MOSFET transistor.

16. (New) A semiconductor device as claimed in Claim 15, wherein a connection region of a drain of the MOSFET borders on the bottom plate and forms a drain connection that projects from the envelope, and wherein connection regions of a source and a gate of the MOSFET are situated on a side of the MOSFET opposite the connection region of the drain, and the first and second conductors form, respectively, source and gate connections that project from the envelope.